We claim:

Sub A1

1. A method of forming a MOS device on a silicon substrate, comprising:

preparing a substrate to contain a conductive region of a first conductivity type having a first device active area;

forming a gate electrode structure on the first device active area, said gate electrode structure including a gate electrode and insulating sidewalls;

implanting ions of an opposite conductivity type from that of said first device active area into the exposed portions of said conductive region to form source and drain regions on opposite sides of said gate structure; and

depositing by selective CVD a silicide layer over said source and drain regions and over said gate electrode.

2. The method of claim 1 in which said implanting step includes implanting ions using plasma immersion ion implantation at an energy in a range of about 0.5 keV to 2 keV.

3. The method of claim 1 in which said implanting step includes implanting ions using plasma immersion ion implantation and includes implanting at a dose in a range of about 1.0×10^{14} cm^{-2} to 1.0×10^{15} cm^{-2}.

4. The method of claim 1 in which said implanting step includes implanting ions using plasma immersion ion implantation and includes implanting to yield a surface ion concentration in said source and drain regions in a range of about 1.0×10^{19} cm^{-3} to 1.0×10^{22} cm^{-3}.

5. The method of claim 1 including, following said step of depositing a silicide layer by CVD, the steps of depositing an insulating layer over the structure and metallizing the structure.

6. A method of forming a MOS device on a silicon substrate, comprising:

preparing a substrate to contain a conductive region of a first conductivity type having a first device active area;

forming a gate electrode on the first active area;

implanting ions of an opposite conductivity type from that of said first device active area into the exposed portions of said conductive region to form source and drain regions on opposite sides of said gate electrode;

forming gate sidewalls adjacent said gate electrode; and

depositing by CVD a silicide layer over said source and drain regions and over said gate electrode.

7. The method of claim 6 in which said implanting step includes implanting ions using low energy ion implantation at an energy in a range of about 0.5 keV to 10 keV.

8. The method of claim 6 in which said implanting step includes implanting ions using low energy ion implantation and includes implanting at a dose in a range of about 1.0×10^{14} cm^{-2} to 1.0×10^{15} cm^{-2}.

Sub A1

9. The method of claim 6 in which said implanting step includes implanting ions using low energy ion implantation and includes implanting to yield a surface ion concentration in said source and drain regions in a range of about 1.0×10^{19} cm^{-3} to 1.0×10^{22} cm^{-3}.

10. The method of claim 6 including, following said step of depositing a silicide layer by CVD, the steps of depositing an insulating layer over the structure and metallizing the structure.

Sub A'

11. A method of forming a CMOS device on a silicon substrate, comprising:

preparing a substrate to contain a conductive region of a first type having a first device active area therein, and to contain a conductive region of a second type having a second device active area therein;

forming gate electrodes on the first and on the second active areas;

depositing and forming a gate electrode sidewall insulator layer on each gate electrode;

masking the first device active area;

implanting ions of a first type into the exposed portions of the second device active area to form a source region and a drain region in the second device active area;

stripping the mask;

masking the second device active area;

implanting ions of a second type into the exposed portions of the first device active area to form a source region and a drain region in the first device active area;

stripping the mask; and

depositing a silicide layer over the gate electrodes and the source and drain regions in the first and second device active areas.

12. The method of claim 11 wherein said implanting steps includes implanting ions using plasma immersion ion implantation.

13. The method of claim 12 wherein said implanting step includes implanting at an energy level in a range of between about 0.5 keV and 2 keV and a dose in a range of between about $1.0x10^{14}$ cm^{-2} to $1.0x10^{15}$ cm^{-2}.

14. The method of claim 12 wherein said implanting step includes implanting to yield a surface ion concentration in said source and drain regions in a range of about $1.0x10^{19}$ cm^{-3} to $1.0x10^{22}$ cm^{-3}.

15. The method of claim 11 wherein said step of depositing a silicide layer includes depositing a silicide layer by selective CVD of silicide.

16. The method of claim 11 including, following said step of depositing a silicide layer, the steps of depositing an insulating layer over the structure and metallizing the structure.

Sub A4

17. A method of forming a CMOS device on a silicon substrate, comprising:

preparing a substrate to contain a conductive region of a first type having a first device active area therein, and to contain a conductive region of a second type having a second device active area therein;

forming gate electrodes on the first and on the second active areas;

masking the first device active area;

implanting ions of a first type into the exposed portions of the second device active area to form a source region and a drain region in the second device active area;

stripping the mask;

masking the second device active area;

implanting ions of a second type into the exposed portions of the first device active area to form a source region and a drain region in the first device active area;

stripping the mask;

depositing and forming a gate electrode sidewall insulator layer on each gate electrode; and

depositing a silicide layer over the gate electrodes and the exposed surfaces of the source and drain regions in the first and second device active areas.

Sub A1

18. The method of claim 17 wherein said implanting steps includes implanting ions using low energy ion implantation.

19. The method of claim 17 wherein said implanting step includes implanting at an energy level in a range of between about 0.5 keV and 10 keV and a dose in a range of between about $1.0x10^{14}$ cm^{-2} to $1.0x10^{15}$ cm^{-2}.

20. The method of claim 17 wherein said implanting step includes implanting to yield a surface ion concentration in said source and drain regions in a range of about $1.0x10^{19}$ cm^{-2} to $1.0x10^{22}$ cm^{-2}.

21. The method of claim 17 wherein said step of depositing a silicide layer includes depositing a silicide layer by selective CVD of silicide.

22. The method of claim 17 including, following said step of depositing a silicide layer, the steps of depositing an insulating layer over the structure and metallizing the structure.